10.7 Low-Power mm-Wave Components up to 104GHz in 90nm CMOS

Babak Heydari, Mounir Bohsali, Ehsan Adabi, Ali M. Niknejad

University of California, Berkeley, CA

Interest in the utilization of the mm-wave band has recently spurred extensive research in the exploration of SiGe and CMOS technologies for high-data-rate short-range communication. Building blocks and complete transceivers have been demonstrated in the 60-to-77GHz range [1, 2]. With the continued scaling of nanoscale CMOS technology and the resulting increase in intrinsic device f_t, there are new opportunities for circuits operating above 100GHz. New potential applications include mm-wave imaging and sub-THz chemical detectors, which have applications in astronomy, chemistry, physics, medicine, and security. In this paper, the operating limits of a digital 90nm CMOS process at both device and circuit levels are explored.

While device scaling results in improved intrinsic unity gain frequency, the actual performance of a device is highly layout dependent. In particular, extrinsic parasitics such as gate, source, and substrate resistance and feedback capacitance are the ultimate factors in determining the maximum frequency of activity (f_{max}). To reduce important external parasitics, the array layout shown in Fig. 10.7.1, dubbed the "round-table" layout, is preferred over a traditional multi-finger FET device. Each sub-element consists of 10 fingers of a double-contacted 1µm-wide device. These elements are connected, as shown in the figure. To minimize parasitics, a multitude of contacts are used at the gate and source terminals. The measured and de-embedded S-parameters and data-fitted small-signal model of the device clearly demonstrate an improvement in the gain of the device. Compared to the standard layout, a maximum standard gain (MSG) improvement of 1dB is obtained. As the device is conditionally stable in this range, a better metric is the unilateral gain/f_{max}, as the device loss is obscured by the external port losses added to stabilize the device. The extrapolated f_{max} of the device is 300GHz, whereas the actual cross-over frequency, predicted by an accurate small-signal model, occurs at 200GHz. This is substantially higher than the f_{max} of the standard layout device (140GHz). This new layout also compares favorably to 0.13µm devices, with measured f_{max} of 135GHz [3]. An extended BSIM3 model is used to capture the device behavior over a wide frequency range [4].

The 40µm round-table device forms the core of a 2-stage 60GHz amplifier shown schematically in Fig. 10.7.2. Since the device is only conditionally stable, the matching network is carefully designed to produce an unconditionally stable amplifier matched to 50Ω. As evident in the layout, coplanar transmission lines are used extensively in the matching and interconnection networks. The two top metal layers are strapped to form the transmission lines and inductive quality factors as high as 30 are measured. All capacitors are realized using dense finger capacitor arrays of strapped metal layers. Custom models are employed for all active and passive devices. The chip is fabricated in a digital CMOS process and no analog options are employed. The on-wafer measured S-parameters (Fig. 10.7.3) demonstrate good input/output matching while driving the pads (not de-embedded). The amplifier has 12dB of gain and consumes 10.4mW from a 1V supply. The measured output 1-dB compression point is +4dBm, resulting in a power efficiency of 24%, which make the amplifier suitable for a pre-driver or PA. The simulated noise figure is 6dB based on extracted noise models from measurements. Compared to previous designs, conditionally stable devices are employed for improved noise performance. The overall power consumption is lower than that of previously reported 60GHz amplifiers [3][5].

A 50µm common-source device is incorporated into a 3-stage 104GHz amplifier. The die micrograph is shown in Fig. 10.7.4. The amplifier utilizes many of the same techniques for matching and biasing. The design is based entirely on measured data of transistors rather than compact models. Passive devices are modeled based on measurements up to 40GHz. Measured S-parameters (Fig. 10.7.5) demonstrate a good input match, 9.3dB of gain, and a reasonable output match. The amplifier consumes 22mW from a 1V supply and clearly demonstrates the potential for CMOS for sub-THz applications.

A 104GHz oscillator is also designed with the 40µm device. The oscillator is based on the Colpitts common-drain capacitive-feedback oscillator in order to provide LO buffering capability in cascode configuration. Simulations of various alternative topologies are performed in order to determine the configuration with high negative resistance per unit current. The Colpitts compared favorably to the ubiquitous differential cross-coupled pair. Furthermore, the output power of the Colpitts is found to be higher than other topologies. A high-quality transmission line inductor (Q ~ 30) resonates with the feedback capacitors and device intrinsic capacitance at 104GHz. The device is biased directly at the gate while the source is grounded through a loop inductor. A loop inductor "choke" (Q ~ 20) in place of a current source allows one to tune out parasitics at this node and boost the negative resistance at high frequencies. Ideally the gate is grounded through on-chip bypass capacitors but available capacitors are insufficiently large to produce a good RF ground, so the capacitance is included in the design of the series resonant tank.

The measured output spectrum clearly shows a strong oscillation at the intended frequency with output power of -8dBm at 104GHz while consuming 6mW (Fig. 10.7.6). While the spectrum analyzer is calibrated for an accurate power reading, the losses in the probe and pad cannot be accurately de-embedded and so the actual output power is -5dBm. High output power is particularly important in mm-wave applications where a strong LO signal is needed to maximize the conversion gain in the mixer. Previously reported W-band oscillators consume more power and deliver less output power [6][7]. While no explicit varactors are introduced, the frequency can be tuned 3% by varying the supply voltage. Phase noise measurements are not performed since the oscillator spectrum is marred by noise and spurious tones. The origin of the tones is related to low-frequency instability and noise coupling as the measurements are made on wafer without sufficient bypass capacitors. The simulated phase noise is -70dBc/Hz at 1MHz offset from the carrier. This oscillator can form the core of a differential VCO with a current-sharing cascode buffer.

Acknowledgements:
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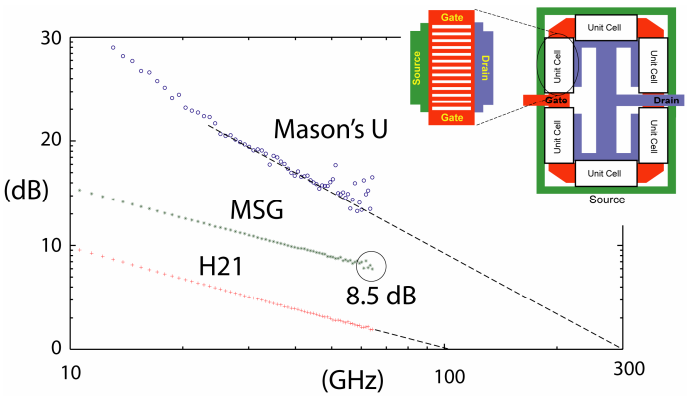

Figure 10.7.1: Measured current gain, maximum stable gain, and Mason's unilateral gain for "round-table" layout transistor.

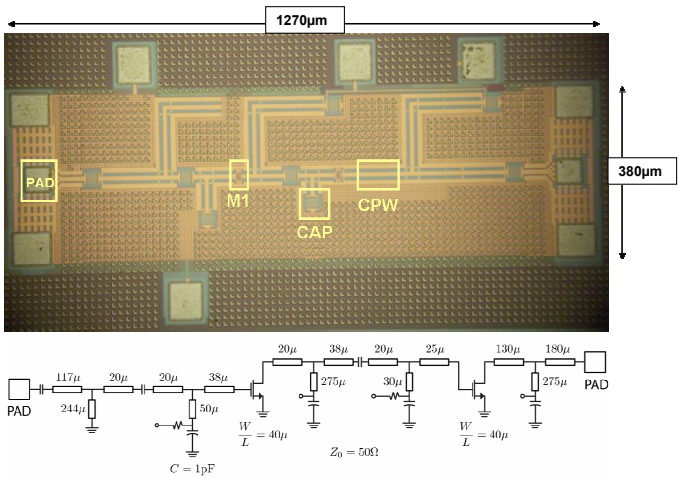

Figure 10.7.2: Die micrograph and schematic of the 2-stage 60GHz amplifier.

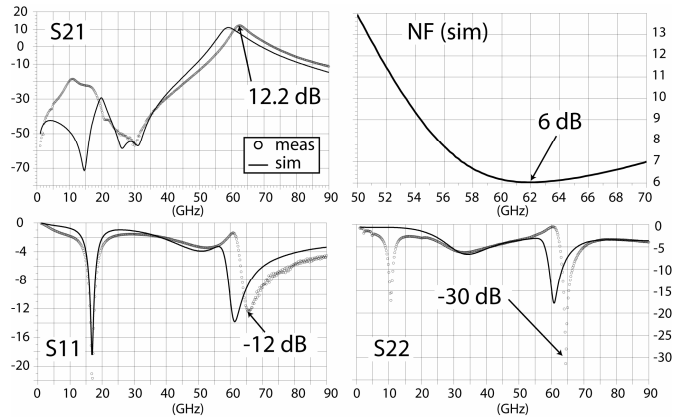

Figure 10.7.3: Measured and simulated performance of the 60GHz amplifier.

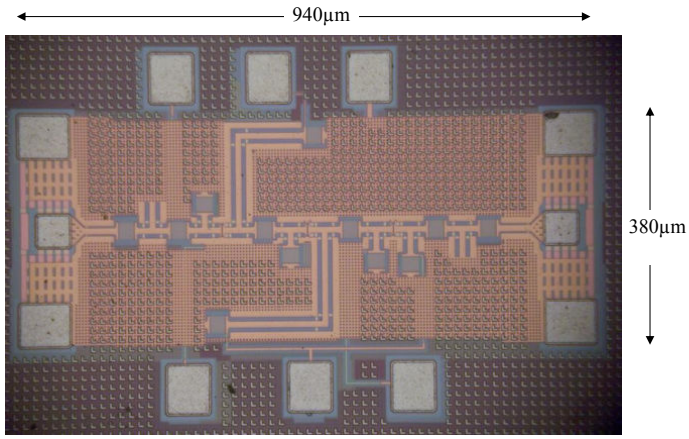

Figure 10.7.4: Die micrograph of the 3-stage 104GHz amplifier.

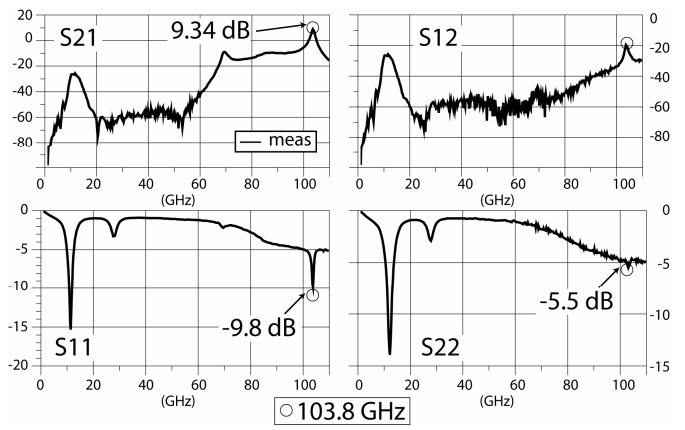

Figure 10.7.5: Measured performance of the 104GHz amplifier.

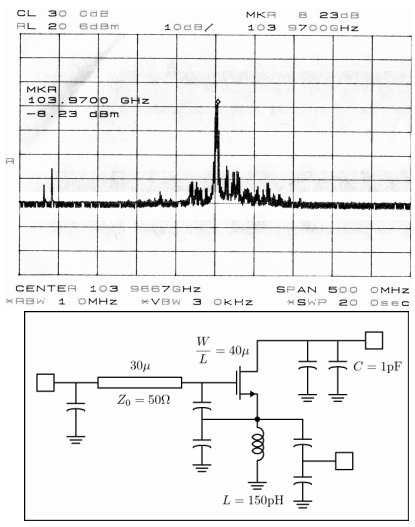

Figure 10.7.6: Schematic and measured output spectrum of the 104GHz Colpitts oscillator.

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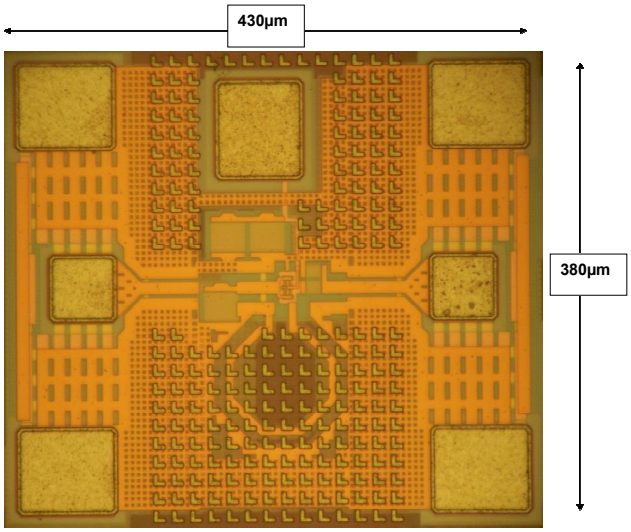

Figure 10.7.7: Die micrograph of the 104GHz Colpitts oscillator.

